GAW Electronics: test of synchronism and simultaneous acquisition

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1. The objective

The purpose of this test is to prove the eligibility of GAW's electronics to compose an array of acquisition modules capable of identifying, capturing and storing rapid events such as those produced by "cherenkov radiation" phenomena.

Specifically, the test focuses on the characteristics that an array of such modules must have to meet the essential requirement of **simultaneity**.

To meet this requirement, it is first and foremost necessary that all modules forming the array are capable of sampling events in synchronism and in phase with a sub-nanosecond accuracy.

In addition, all array modules have to produce a timeline window, for event acquisition, that pursues the same accuracy as mentioned before.

Finally, the array must be able to produce a stand-alone events trigger, in which each module contributes with its own information to shape a global event-identification trigger, by virtue of a temporal alignment of this information to the sub-nanosecond.

In particular, all of these properties must be insensitive to the different lengths and characteristics of the cables connecting the array modules.

2. Specifications

To implement the functionality mentioned above is therefore essential to:

- 1) Distribute a CLOCK signal common to all the modules forming the array, crucial to performing the required synchronous sampling
- 2) Carefully align the CLOCK phase for each module
- 3) Distribute a STROBE signal common to all the modules that form the array, indispensable to creating a common acquisition timeline window between all the modules
- 4) Implement a precise STROBE time alignment
- 5) Collect TRIGGER signals from each module to form a global trigger for event identification
- 6) Make a precise temporal alignment of TRIGGER signals

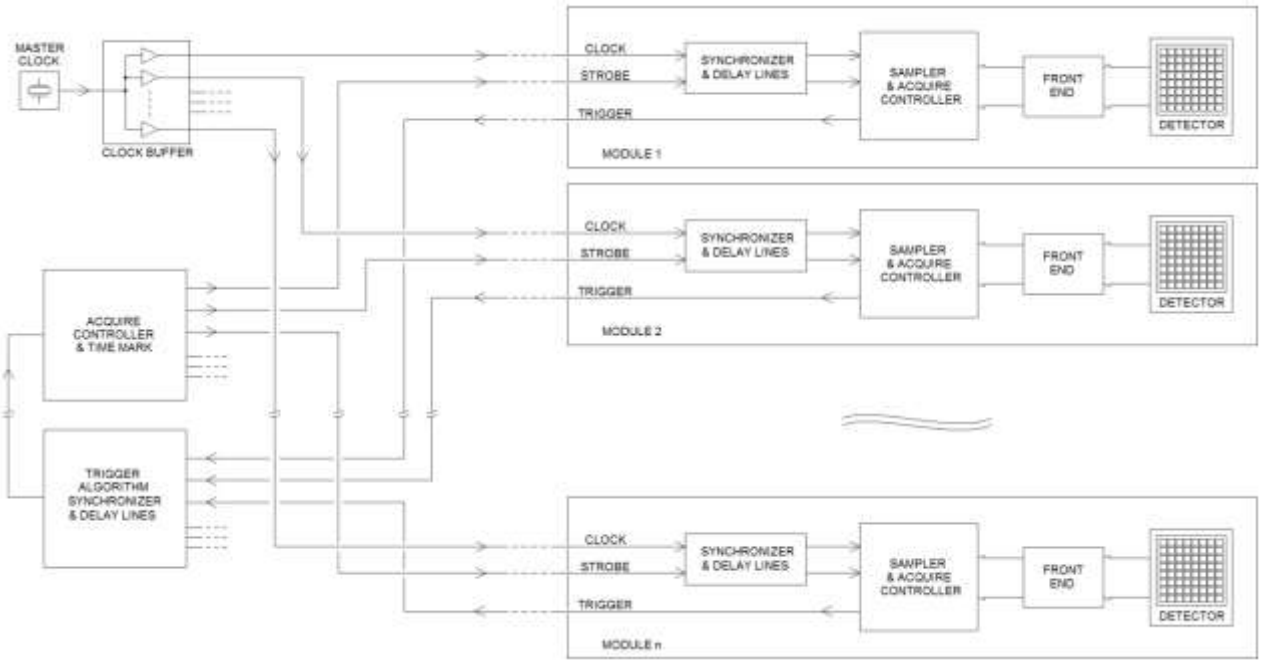


Figure 1. Typical configuration of an array of capture modules, and related connections of the major synchronization signals

Obviously, along with the above-described signals (Figure 1), I/O signals must be distributed for interfacing with all the array modules, considering that for large arrays it is desirable to have an high data rate, in order to minimize the dead time on scientific data reading.

3. The acquisition module

Insisting on the scope covered by the purpose of this test, it is only important to note that each acquisition module developed for GAW project (Figures 2 and 3) is capable of sampling at 200MHz, on a cyclical memory deep 10us, 256 Digital signals + 4 analog signals, coming from the front-end of the detectors. In addition, there is an event handler integrated into it, which, promptly transfers them into a dual buffer storage memory at the end of the acquisition window, in order to minimize the reading dead time. The acquisition window ends when the STROBE signal arrives following the identification of the event to be captured.

Figure 2. A row of 3 adjacent acquisition modules, in a 3 x 3 focal plane

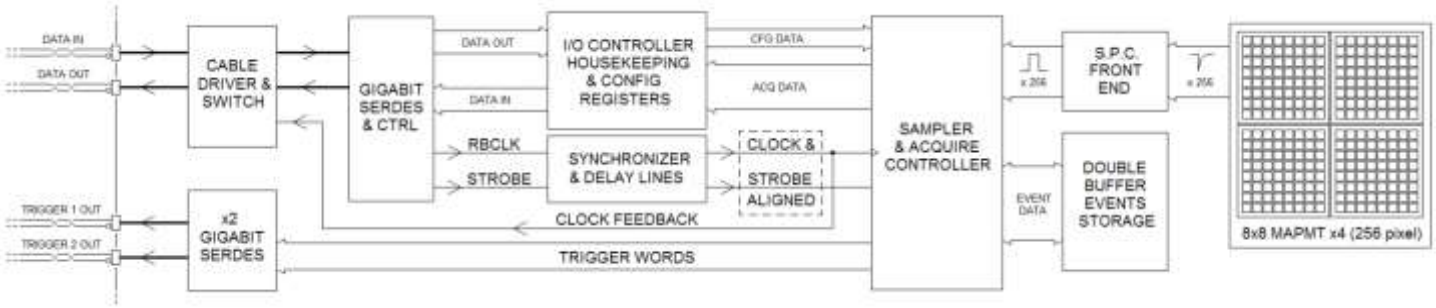


Figure 3. Block diagram of an acquisition module

4. The mother unit

Regarding GAW electronics, a distribution and collection unit has been developed for all the necessary connections and functions, both towards to the acquisition modules and to a main processor. This "mother" unit (Figures 4, 5 and 6), although it can support a limited number of capture modules (up to 12 units in this version), is also designed to allow large array management, thanks to the intrinsic possibility In its design to make a hierarchical tree interconnection with other identical mother units (Figure 7). In order

to optimize design effort, the motherboard has been structured modularly. It consists essentially of three types of modules: one or more “master” modules, a “l-control” module, and a “trigger” module.

Regarding the type of connection used, the design path adopted intends to meet all the required interfacing and synchronization specifications, through a simple and economical means of transport such as the ethernet cable. This choice obviously represents a challenge observing the small number of lines in this cable, which correspond only to 4 twisted pairs.

In fact, each acquisition module is connected to the mother unit through only one ethernet cable that transfers data, synchronisms and triggers in compliance with the specifications mentioned.

Figure 4. The mother unit equipped with 10 master modules, the l-control module and the trigger module

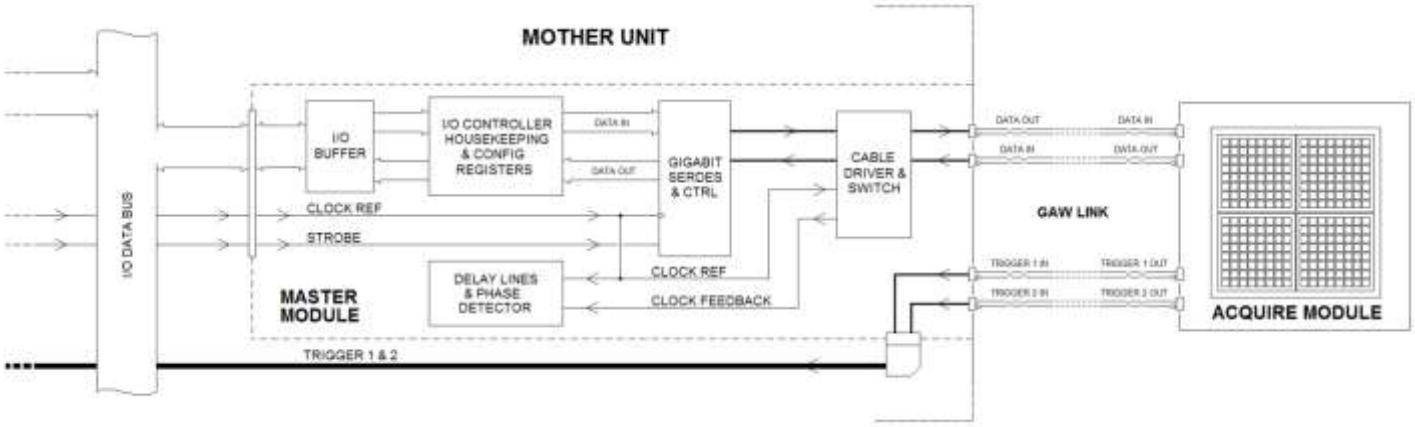


Figure 5. Block diagram of a master module in the mother unit, connected to the acquisition module

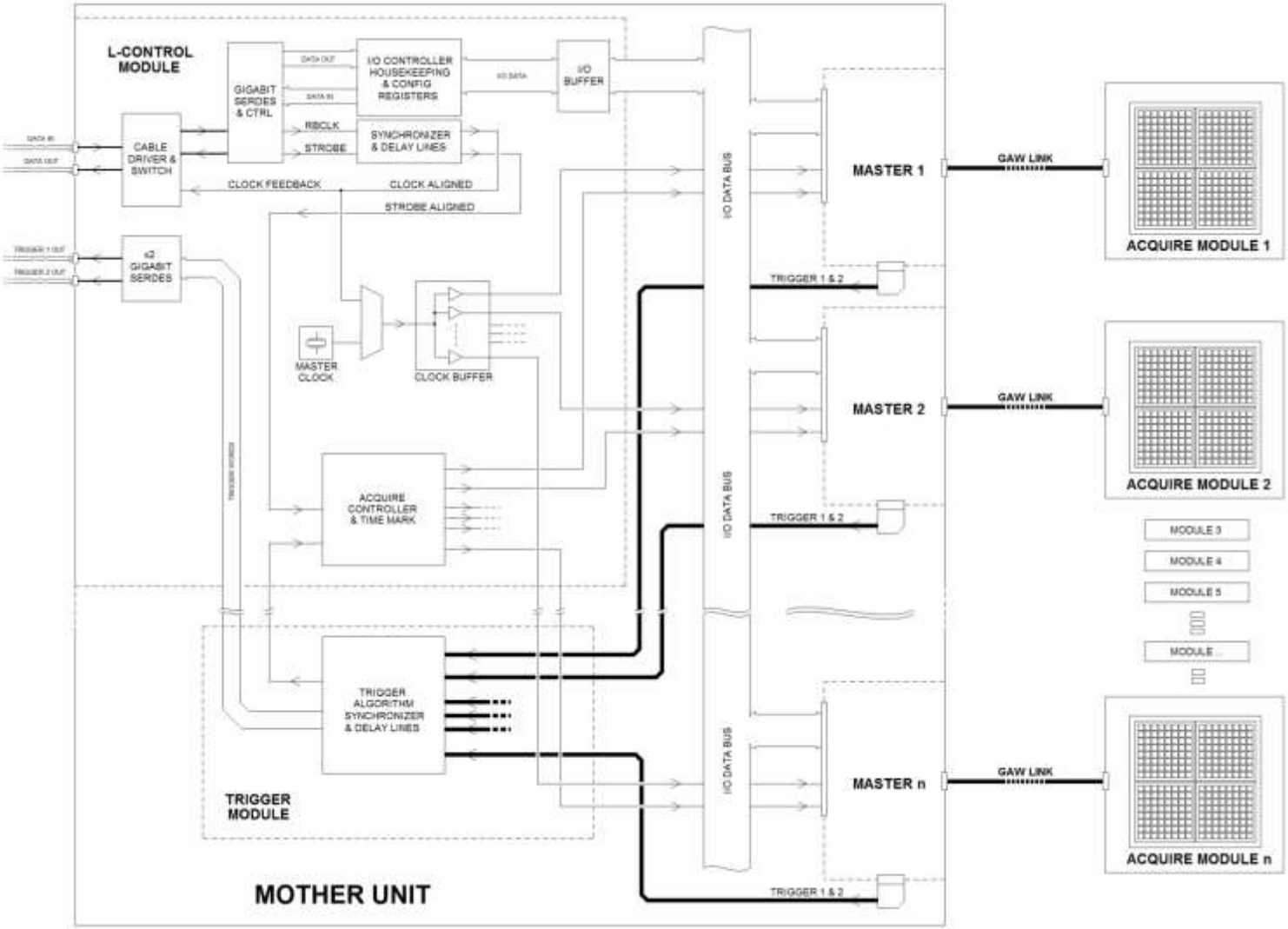


Figure 6. Block diagram of the mother unit connected to the acquisition modules

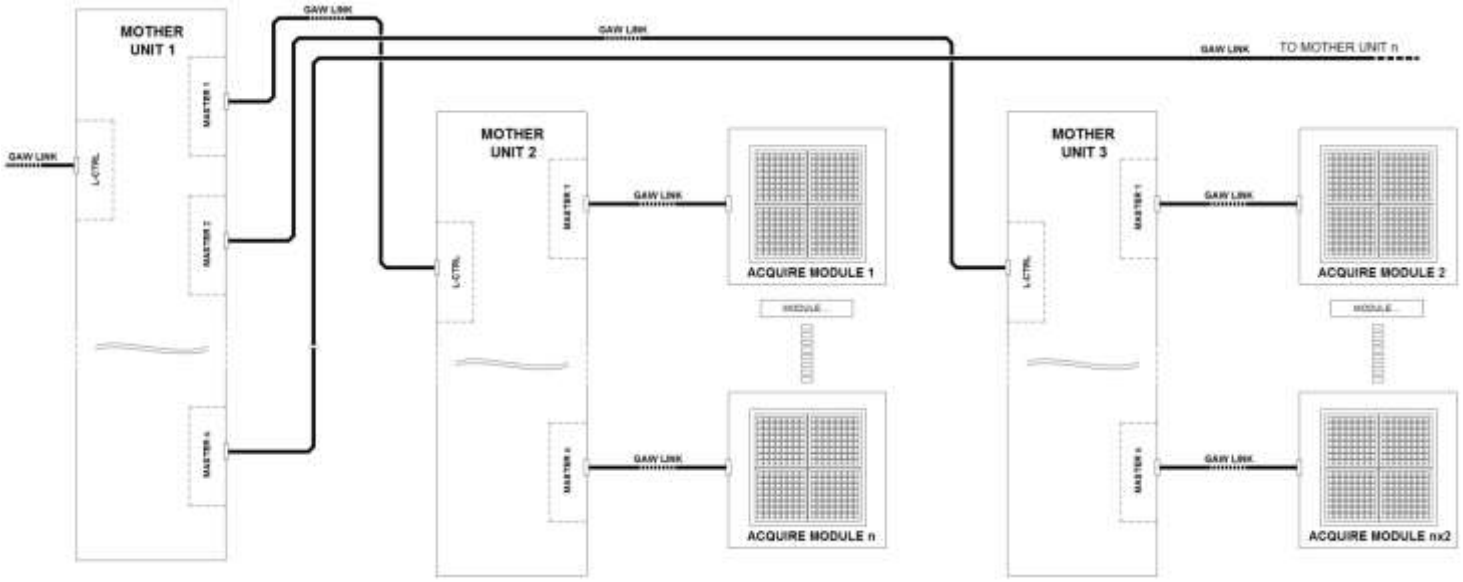


Figure 7. Configuration of multiple tree-related mother units

5. Connections

In the GAW mother unit, each connecting path is conceived as follows:

- Line 1: I/O data output
- Line 2: I/O data input
- Line 3: trigger data input 1
- Line 4: trigger data input 2

Each of these lines adopts an high-speed (2Gbit / sec) gigabit serial connection, which secures a transmission with a maximum data rate of 200MB / sec for each line.

To do this, extensive use of high-speed "SerDes" serial devices has been made, enabling easy and effective physical-level management of the connection and transmission of the required data.

For the management of I/O data transmission, a proprietary firmware protocol has been developed and widely tested, which guarantees an high degree of efficiency and security. The main features of this protocol are the following:

- Low latency double I/O buffer
- Reconfigurable commands, status, package length and parameters
- CRC on CMD, DATE and STATUS
- Error handling with automatic retransmission of data
- Handshake with adaptive timing

Additionally, within the protocol, an essential feature was added to allow STROBE signal distribution throughout the array: the mode called ACQUIRE (see paragraph 9).

For the transmission of TRIGGER information (needed to identify events to capture), it was chosen a simple streaming mode for data management, with configurable error filtering. It is thought to treat this data flow

as a video data stream, where transmission speed is a priority over an intolerance on transmission errors. In this case, these errors would only produce false evaluations of possible triggers.

6. The I/O interface

Thanks to a special I/O interface, the mother unit is detected by any computer as a common data storage device. This interface (Figures 8 and 9) consists essentially of a DELPHIN board connected, through its own reconfigurable local-bus, to a gigabit SerDes device which can be connected in turn to the mother unit through both copper cable and optic fiber via SFP modules.

The DELPHIN card is a proprietary board developed before the GAW project and improved over time to constantly adapt it to the latest technologies for interconnection between computers and peripheral devices. Born, initially on SCSI standards, in order to simplify and standardize the interfacing of the many instruments developed over the years by the IASF-PA lab, the board allows the management of the instrumentation connected to it by simple I/O file operations thanks to a proprietary firmware controller able to emulate a common Hard-Disk all over.

Today, the DELPHIN board allows you to interface to a PC through standard USB 2.0 and/or eSATA (USB 3.0 under development) ports, with a current data rate of 100MB/sec (133MB/s max).

Figure 8. I/O interface (left) and the DELPHIN board (top center) integrated into the GAW I/O interface

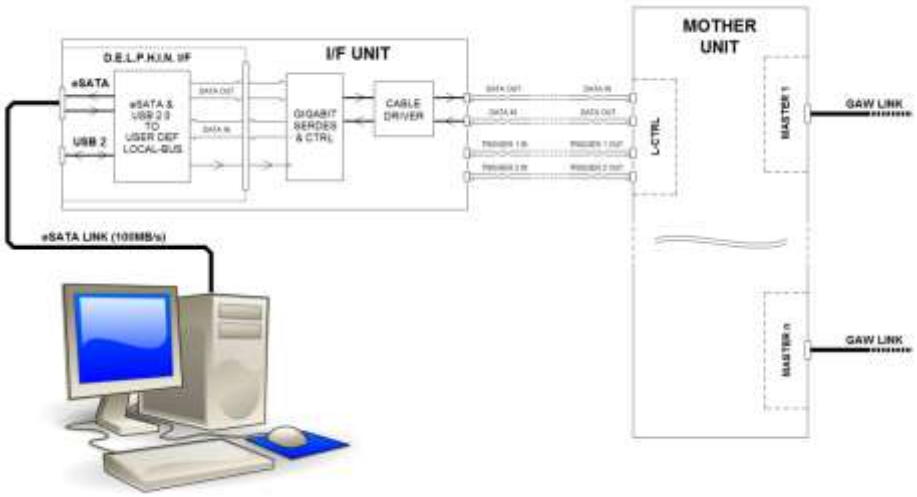


Figure 9. The mother unit connected to a computer through the I/O interface

7. The synchronous clock

Given the small number of lines available in the connecting means used, some stratagems had to be used to meet the basic requirements of the above-mentioned simultaneity.

To achieve the first required functionality, ie the distribution of a synchronous CLOCK signal across the array of modules, it was decided to exploit a peculiar characteristic of all SerDes devices (Figure 10). They need to accurately reconstruct the data source clock from the received gigabit signal to properly decode the incoming serial data. The clock thus reconstructed has the same frequency as the data source clock and is in perfect sync.

In a nutshell, the distribution of a synchronous CLOCK for all array modules is simply obtained using the reconstructed clock signal, which is made available by the SerDes devices present in each capture module.

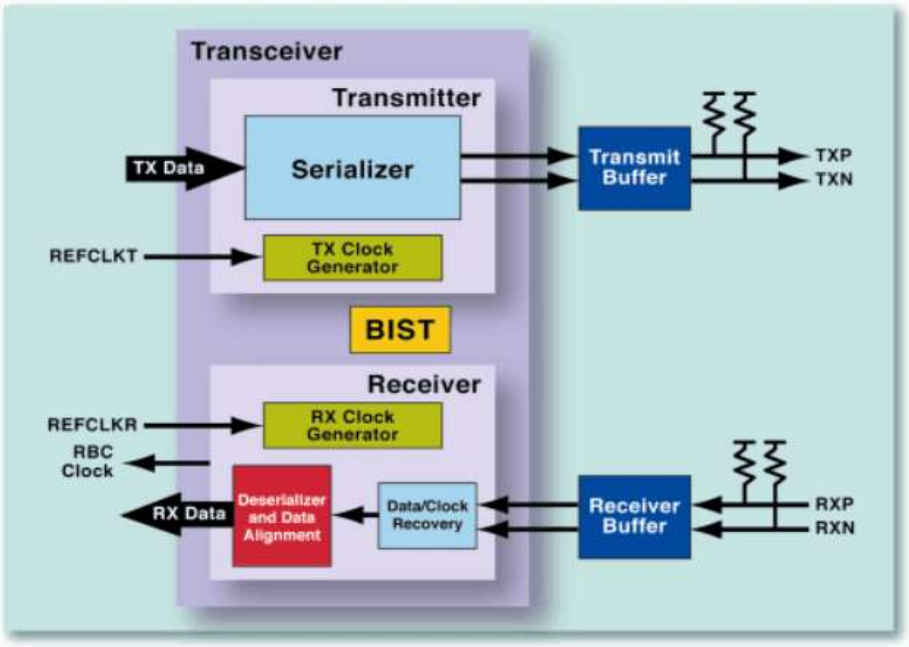
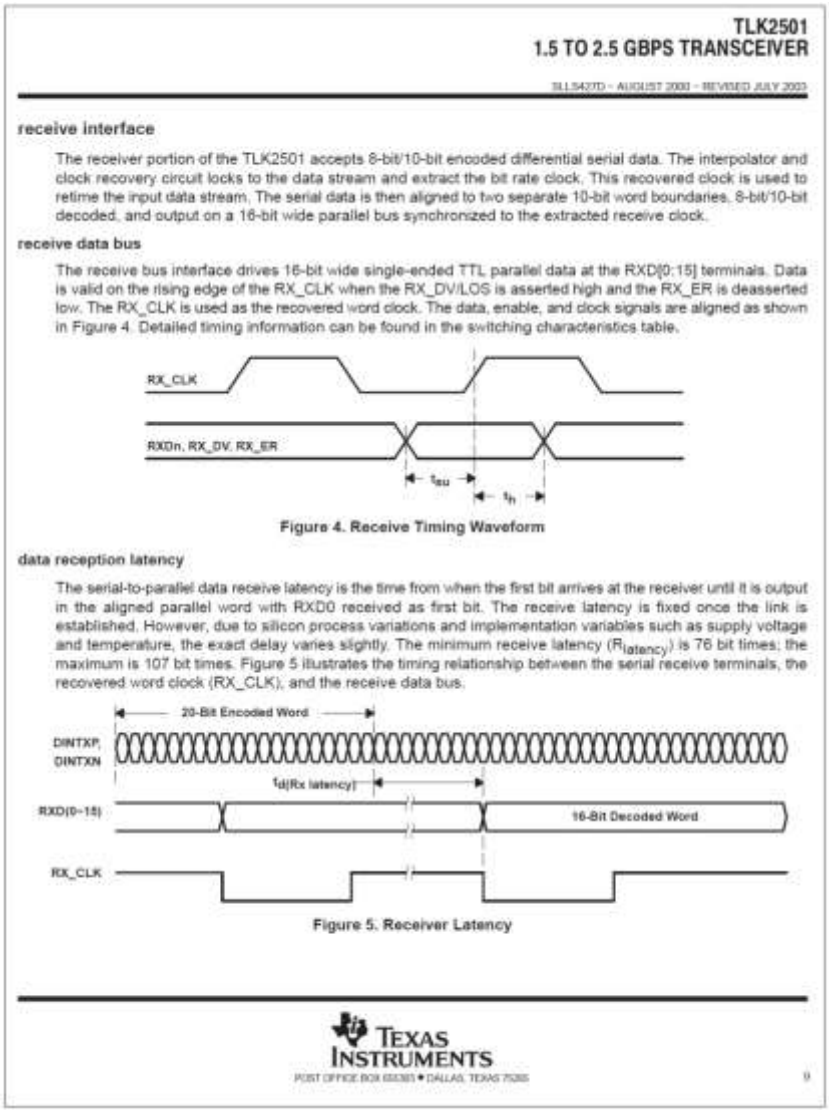


Figure 10. Block diagram of a typical SerDes device

8. … and its alignment

The realization of the second functionality, ie the adjusting of the CLOCK phase throughout the array, unfortunately is not so easy because of the non-predictive latency on clock reconstruction shown by all SerDes devices.

This latency is variable in the order of tens of nanoseconds (Figure 11), and is defined during the synchronization process initially and automatically performed by each SerDes device. Once defined, it remains constant at less than a loss of connection, which necessarily restarts the re-synchronization process.



TLK2501
1.5 TO 2.5 GBPS TRANSCEIVER

SLLS427D – AUGUST 2000 – REVISED JULY 2003

receive interface

The receiver portion of the TLK2501 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit locks to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded, and output on a 16-bit wide parallel bus synchronized to the extracted receive clock.

receive data bus

The receive bus interface drives 16-bit wide single-ended TTL parallel data at the RXD[0:15] terminals. Data is valid on the rising edge of the RX_CLK when the RX_DV/LOS is asserted high and the RX_ER is deasserted low. The RX_CLK is used as the recovered word clock. The data, enable, and clock signals are aligned as shown in Figure 4. Detailed timing information can be found in the switching characteristics table.

Figure 4. Receive Timing Waveform

data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RXD0 received as first bit. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum receive latency ($R_{latency}$) is 76 bit times; the maximum is 107 bit times. Figure 5 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RX_CLK), and the receive data bus.

Figure 5. Receiver Latency

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Figure 11. Description of Texas Inst. SerDes TLK2501 Feature Latency

Because of this latency, it was necessary to create an “ad hoc” hardware circuitry able to compensate for this delay, and thus adjust the CLOCK phase throughout the array with the precision needed.

This circuitry (Figure 12), subdivided in part into the mother unit and partly into the acquire module (Figure 13), allows two essential measurements to be made. The first is the measurement of total propagation delay, round-trip, of the transmission line without the SerDes devices. The second is the same measurement including those devices, but only those on the forward path, from the mother unit to the acquire modules.

With these two measurements it is easy to calculate the one-way forward propagation delay on the transmission line, which is the relevant target for the purposes of the final compensation:

$$Delay\_up = (Delay\_tot\_no\_serdes / 2) + (Delay\_tot\_serdes\_up - Delay\_tot\_no\_serdes)$$

The circuitry consists of high-speed CML, LVPECL and LVDS logic devices (f ≥ 3GHz) with ultra-low JITTER and SKEW, and allows precise measurement and correction of this phase shift with a resolution of 10ps.

As will be seen later, the measurement of the one-way forward propagation delay is also essential to subsequently implement the alignment required for the fourth simultaneity feature: the STROBE time alignment (see paragraph 10).

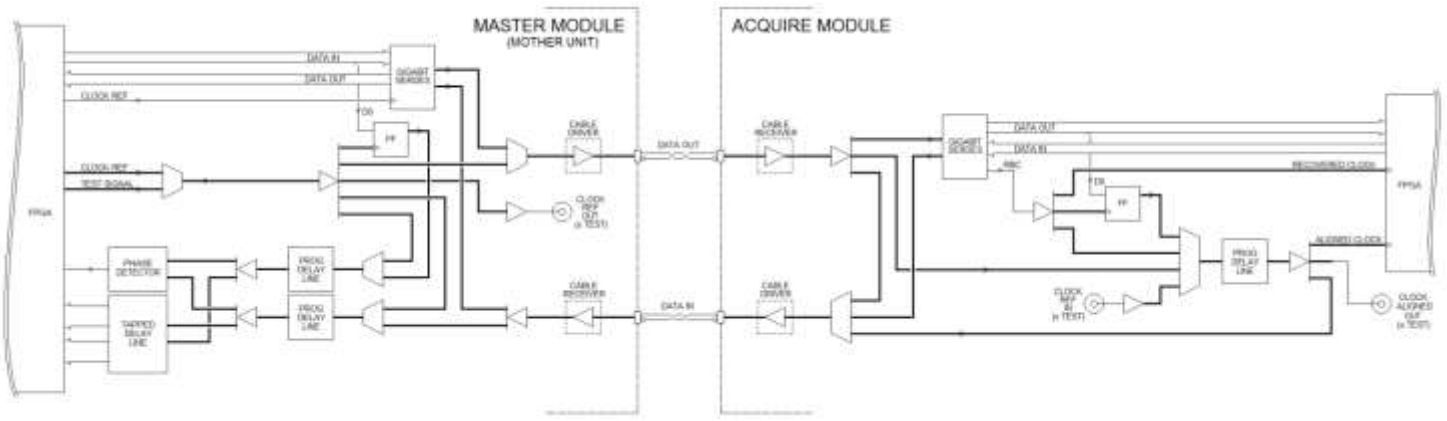

Figure 12. Block diagram of the circuitry used to compensate latency, present in each master module of the mother unit and in the acquisition modules

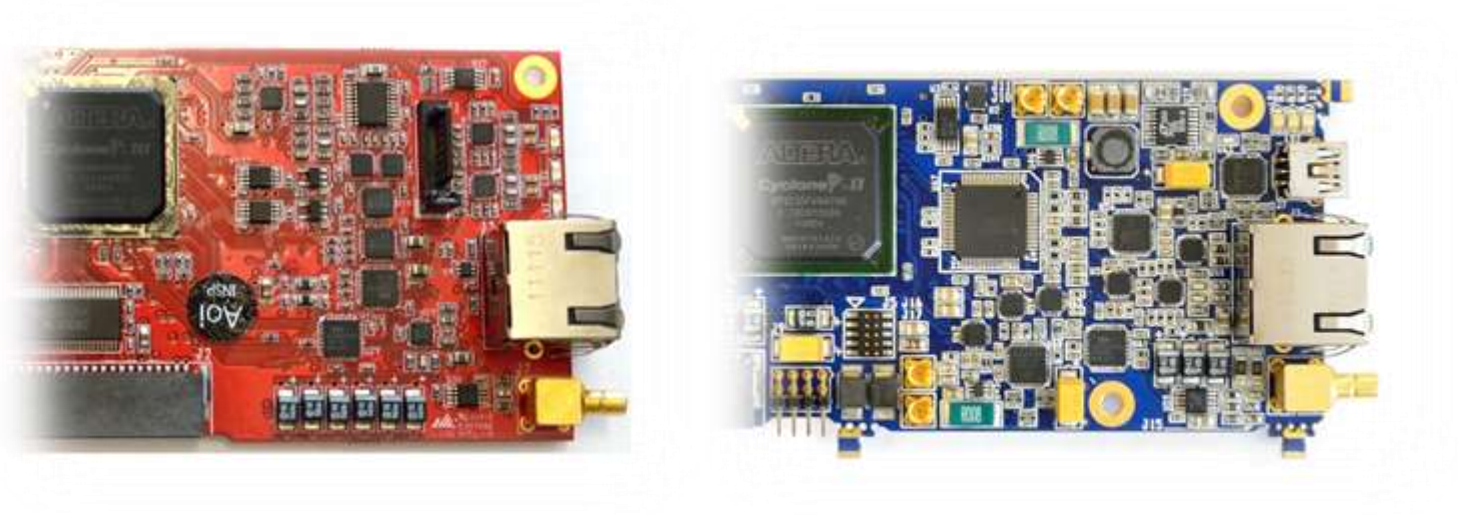

Figure 13. Details of the compensation circuits integrated within the master modules and the l-control section of each acquisition module

9. The strobe

The third feature, ie the distribution of a STROBE signal throughout the array (needed to manage the acquisition timeline window), was obtained by exploiting a particular transmission mode called ACQUIRE, developed specifically in the previously discussed proprietary protocol.

This mode, which can be efficiently exploited only during the process of reading data (scientific, housekeeping or any other type of data), allows mixing together with handshakes directed to acquisition modules and necessary for protocol management some service signals independent of the protocol and manageable by external features.

This mode allows you to send simultaneously and without interruption to all acquisition modules one or more STROBE signals (up to 3) with a resolution equal to the period of the data transmission clock , ie 10ns.

10. … and its alignment

The fourth feature, that is, STROBE time alignment across the array, as previously anticipated, is achieved by the measurement of the one-way forward transmission propagation delay. The measurement is obtained during the CLOCK phase correction procedure, and while the STROBE signal is passed through a suitable programmable digital delay line.

This digital delay line is essentially a dual-port FIFO type firmware memory, in which the clocks of input and output ports are connected respectively to the clock reconstructed by the SerDes device, and to the rephased CLOCK.

In this way, after computing all the global transmission line delays, it is possible to align all distributed STROBE signals with a resolution of 10ns and with the accuracy obtained by the correction process of the reconstructed CLOCK phase previously performed.

11. The trigger

The fifth feature, that is, the TRIGGER signals collection from the entire array, does not need any particular clarification. It is obtained simply by the lines 3 and 4 dedicated to this purpose.

Two 2Gbit / sec lines have been dedicated for this feature so that a 400 MB / sec data stream can be ensured from each capture module. Thus, the processing unit present in the mother unit trigger module receives, every 10ns, 32 bits of information from each capture module completely independent. This flow offers great potential in terms of processing an accurate continuous, fast, and efficient trigger algorithm.

12. … and its alignment

The sixth and last functionality, ie the TRIGGER data flows alignment from all over the array, makes use of digital alignment memories. In the same way as previously explained, all TRIGGER streams received in the mother unit are transmitted through that alignment memory, having careful to:

- Simultaneously start TRIGGER data flow out of all capture modules, using one of the temporally compensated STROBE signals
- Start the algorithm computing process as soon as all TRIGGER streams have reached the mother unit trigger module (Figure 14)

In this way, with a simple artifice, the time alignment of all TRIGGER streams is achieved with the same accuracy and alignment resolution reached for the signals already described above.

Figure 14. The trigger module

13. The set-up

For this demonstration, an experimental set-up was designed (Figures 15 and 16) to simulate a portion of array. The set-up consists of 3 acquisition modules connected to the mother unit through a suitable combination of different wiring, in order to test the system insensitivity to a different typology and length of the connections.

With the help of a LeCroy WaveMaster 808Zi-A (SDA) oscilloscope, the original CLOCK signal coming from the mother unit and the 3 reconstructed and compensated CLOCK signals of the acquisition modules are displayed and monitored thanks to the 4 input channels present.

In addition, by means of the digital input channels in the oscilloscope, the following is displayed: the external STROBE signal produced by an HP 8110A pulse generator but pre-sampled and sent from the mother unit, and the incoming signals in the 3 acquisition modules before and after the programmed digital alignment.

Finally, always through the digital input channels of oscilloscope are introduced and displayed 3 check-up signals extracted from the TRIGGER information flow coming from the modules, the same signals after the time alingment, and the global trigger signal, result of the algorithm operated In the mother unit.

For demonstration purposes, a simple summing algorithm was configured for the TRIGGER information received, submitted then to a majority threshold.

The TRIGGER information outcoming from the 3 modules is alternately enabled by the level of a pulse generated by a second channel of the pulse generator in use, and distributed to the 3 modules through many other NIM Ortec 425A delay modules with 1ns step selectable delay.

All this in order to emulate the arrival in coincidence or not of an event in the array and verify, therefore, the correct time alignment of TRIGGER information.

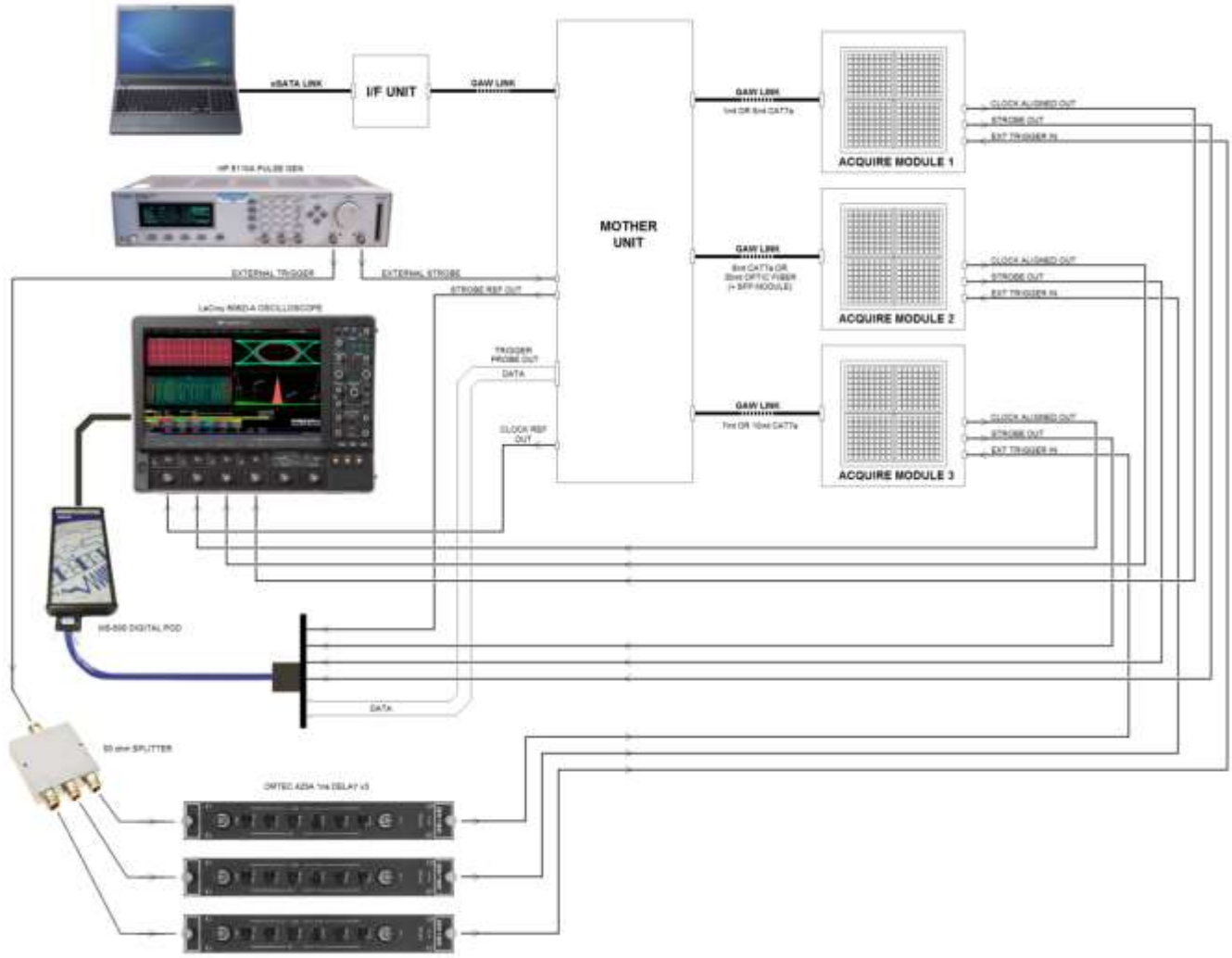

Figure 15. Set-up connection chart

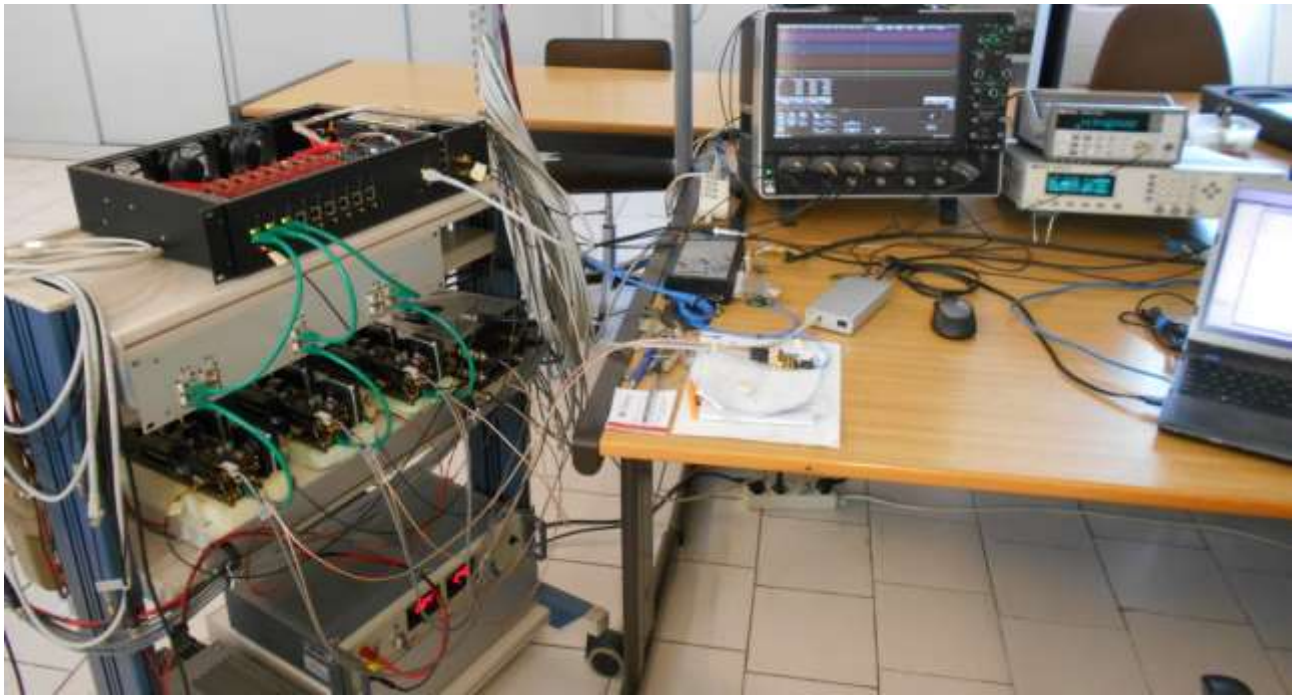

Figure 16. The complete set-up

14. Measures

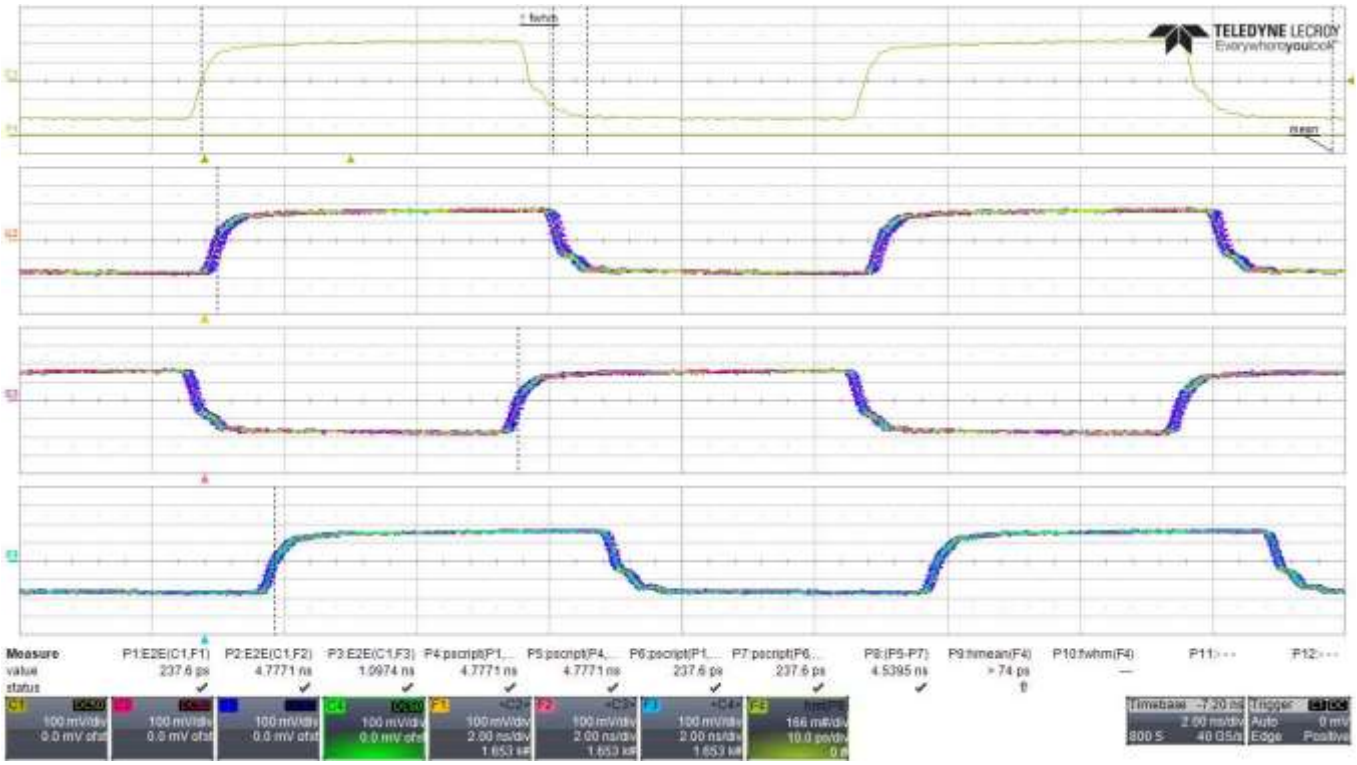

Figure 17. An example of clock signals before phase alignment. CH 1 = clock ref; CH 2-4 = clocks of acquisition modules 1-3

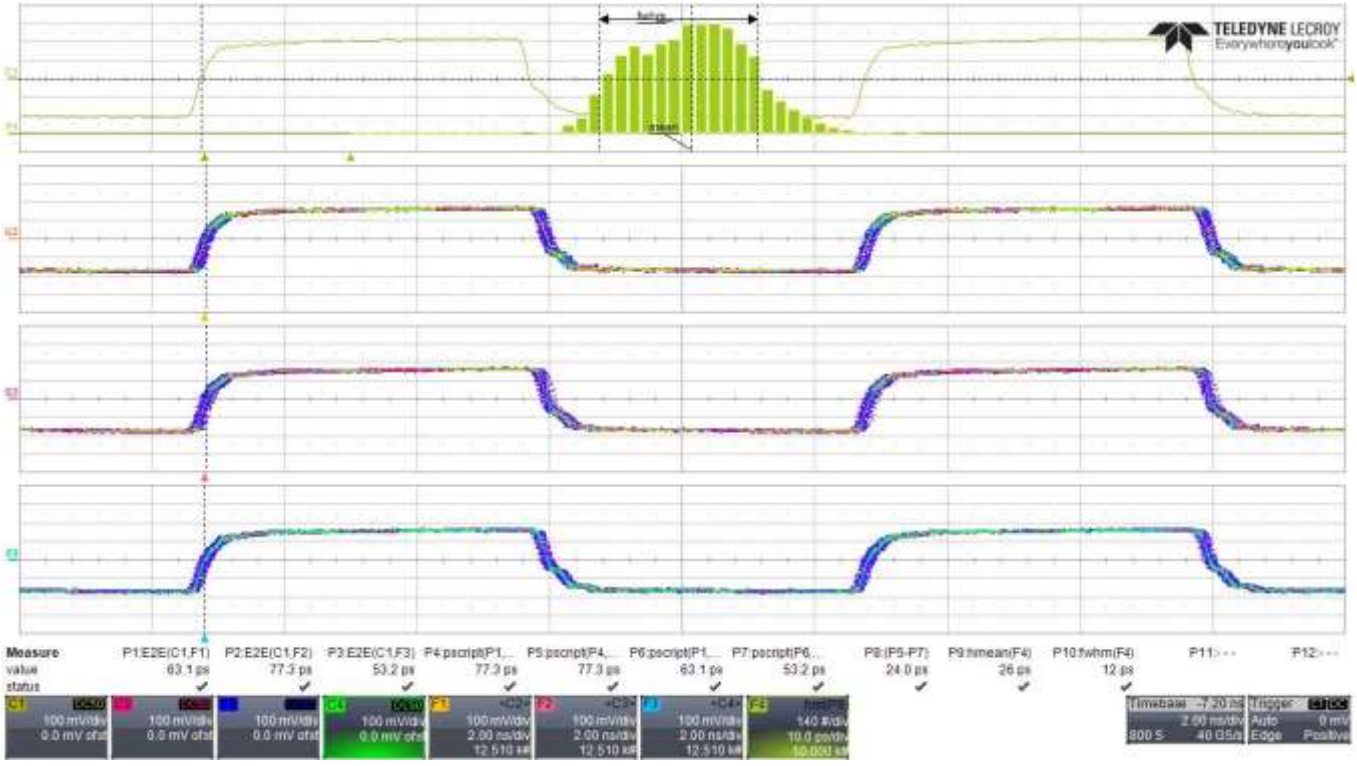

Figure 18. Cables: 5, 6 and 7 mt in length. Clock Alignment: Average = 26ps. FWHM = 12ps

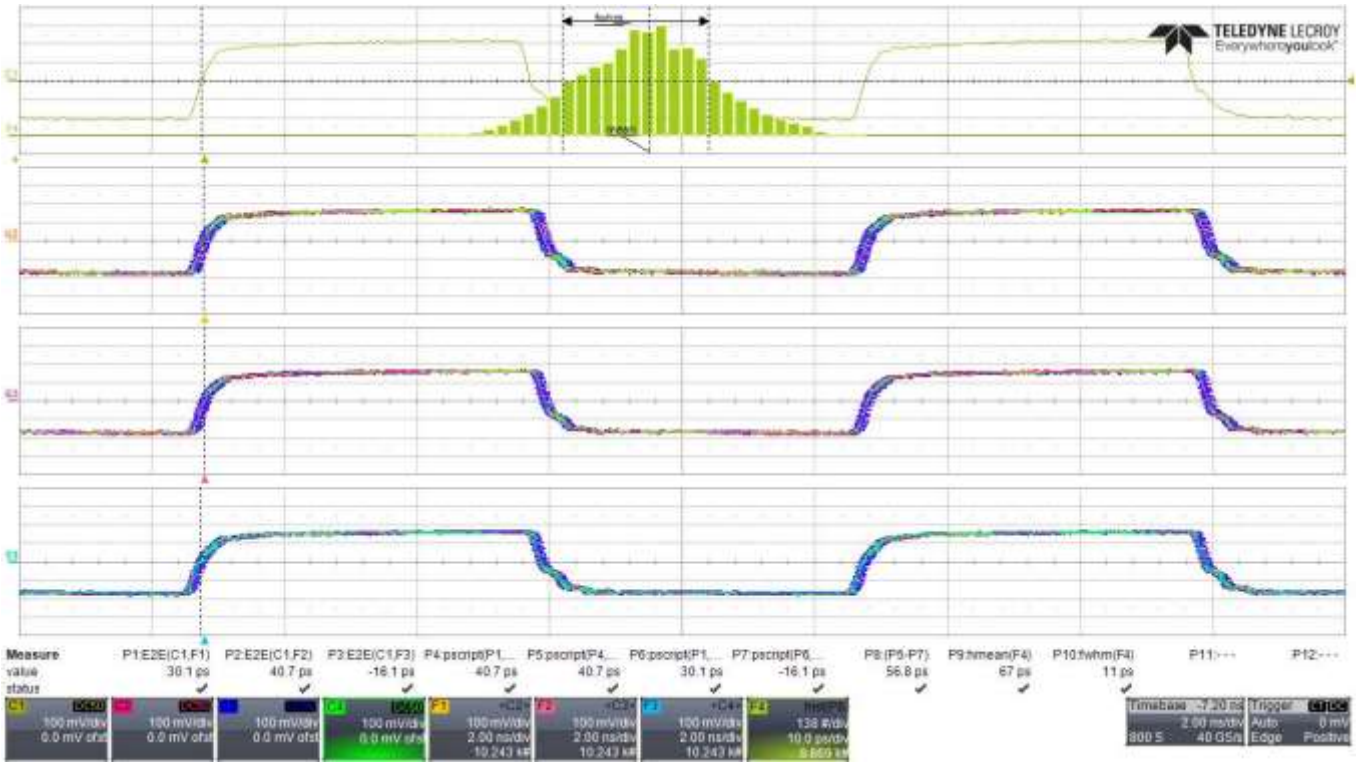

Figure 19. Cables: 1, 6 and 10 mt in length. Clock Alignment: Average = 67ps. FWHM = 11ps

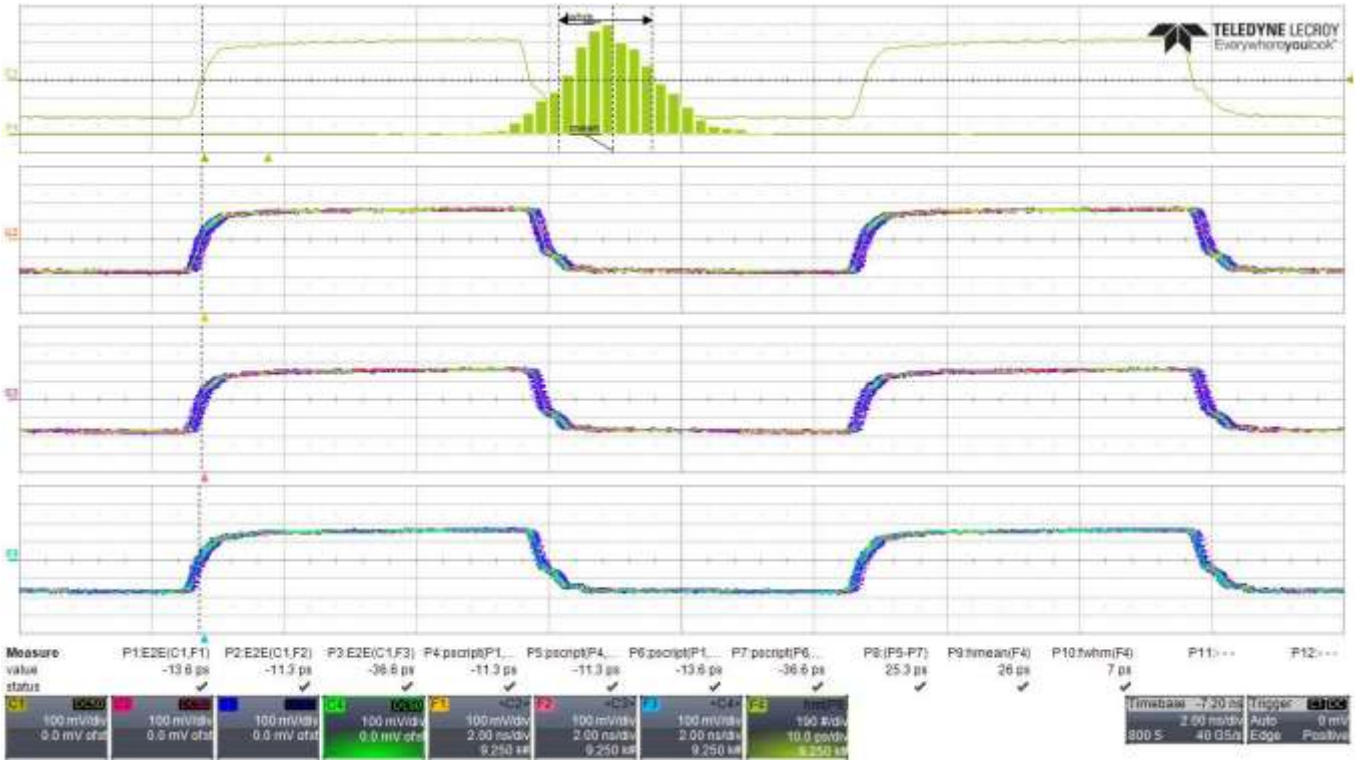

Figure 20. Cables: 1, 30 (optic fiber + SFP) and 10 mt in length. Clock Alignment: Average = 26ps. FWHM = 7ps

Figure 21. Cables: 1, 6 and 10 mt in length. STROBE ref and STROBEs of modules 1-3, before time alignment

Figure 22. Cables: 1, 6 and 10 mt in length. STROBEs of modules 1-3 aligned temporally

Figure 23. Cables: 1, 30 (fiber optic + SFP) and 10 mt in length. STROBEs of modules 1-3 before time alignment

Figure 24. Cables: 1, 30 (fiber optic + SFP) and 10 mt in length. STROBEs of modules 1-3 aligned temporally

Figure 25. Cables: 1, 6 and 10 mt in length. In addition to the aligned STROBEs, the TRIGGER stream check-up signals coming from the modules are added before and after the time alignment. The last down is the global trigger signal that is output from the summation and majority algorithm

Figure 26. It repeats as shown in in Fig. 25 but after the addition of a 32ns delay (via the ortec 425A module) on the TRIGGER enabling of the 3rd module. The absence of the global trigger signal is noticed because of the incorrect temporal coincidence appropriately created

15. Results

It should be noted that during this test phase, no calibration of the circuitry used to temporal compensation of the signals to be measured has been performed.

Despite this, the results obtained are very satisfactory and show a time alignment capability for signals far greater than expected.

In particular, it is noted that by using a quality ethernet cable (type cat7a SF12004SH) with connection lengths of 5, 6 and 7 meters, respectively, with the three modules, the time alignment of the CLOCK takes place within 100ps (max).

Recall that, typically, the propagation delay for these cables is around 5ns per meter.

Increasing the cable length gap between the three modules at 1, 6 and 10 meters respectively, the alignment degrades slightly but keeps within 150ps (max).

In addition, thanks to the gigabit serial connection used, it was also possible to make a optical fiber connection test (Figure 27) with one of the three modules under test. With mixed connections of 1 and 10 meters in copper cat7a and 30 meters in fiber, through AVAGO AFBR-57R5APZ optical SFP modules, the final alignment has always remained within 150ps (max).

This type of optical fiber connection is expected to provide excellent results in terms of time alignment, even for large distances of connection with the modules.

Of course, the performance degrades considerably when using, for connections, types of cable different from each other and/or poor in quality (cat5e and cat6). In this case, the worst alignment measured between the modules does not exceed 1 ns (max).

With this set-up it was also possible to successfully verify the performance of the trigger algorithm implemented in its processing unit.

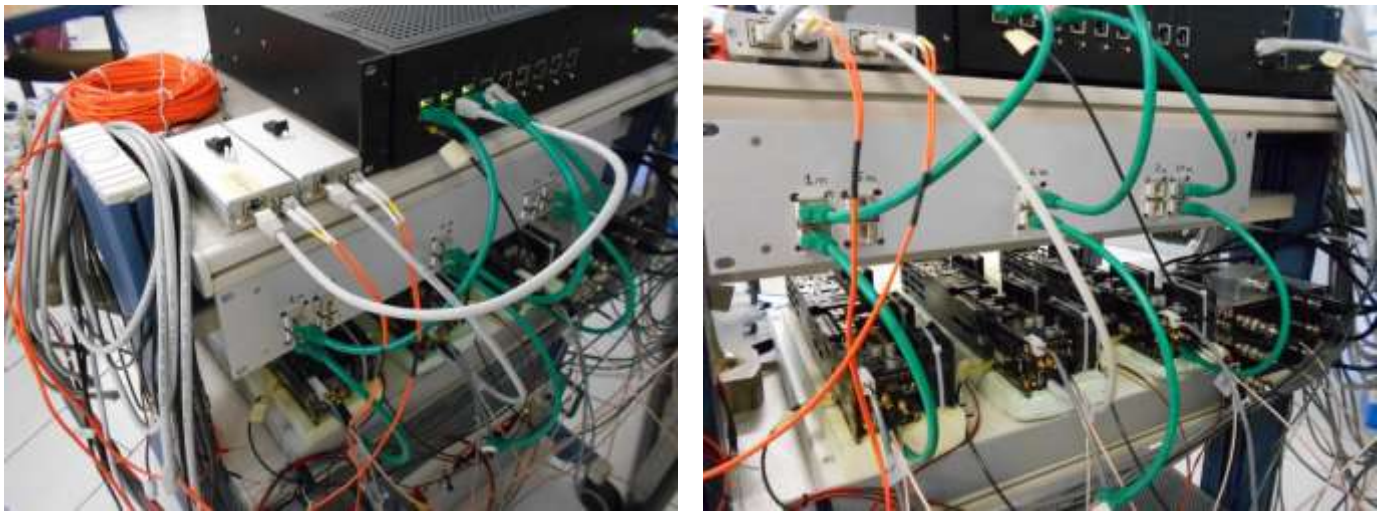

Figure 27. The optical fiber and SFP modules (left). Detail of acquisition modules (right)

16. Conclusions

Similarly to other sub-nanosecond synchronization systems developed more or less in conjunction with this project (roughly with the spread of high-speed SerDes devices), such as CERN's White Rabbit, GAW's synchronization system stands out for the high precision achieved. This test ultimately demonstrates that all the electronics developed for the GAW experiment are suitable for the assumed use in the lens of this exposure. It is therefore able to:

- Perform synchronous and simultaneous sampling on several independent modules, connected to a dedicated mother unit
- Identify the events to be captured autonomously, through a sophisticated global trigger
- Transfer data from experiment to a computer at high-speed, allowing you to minimize acquisition dead time

In perspective, it is possible to say that the management philosophy studied for this electronics could be a useful resource for various types of instrumentation and experiment in which array formation or the relocation of measurement devices operating simultaneously are required.

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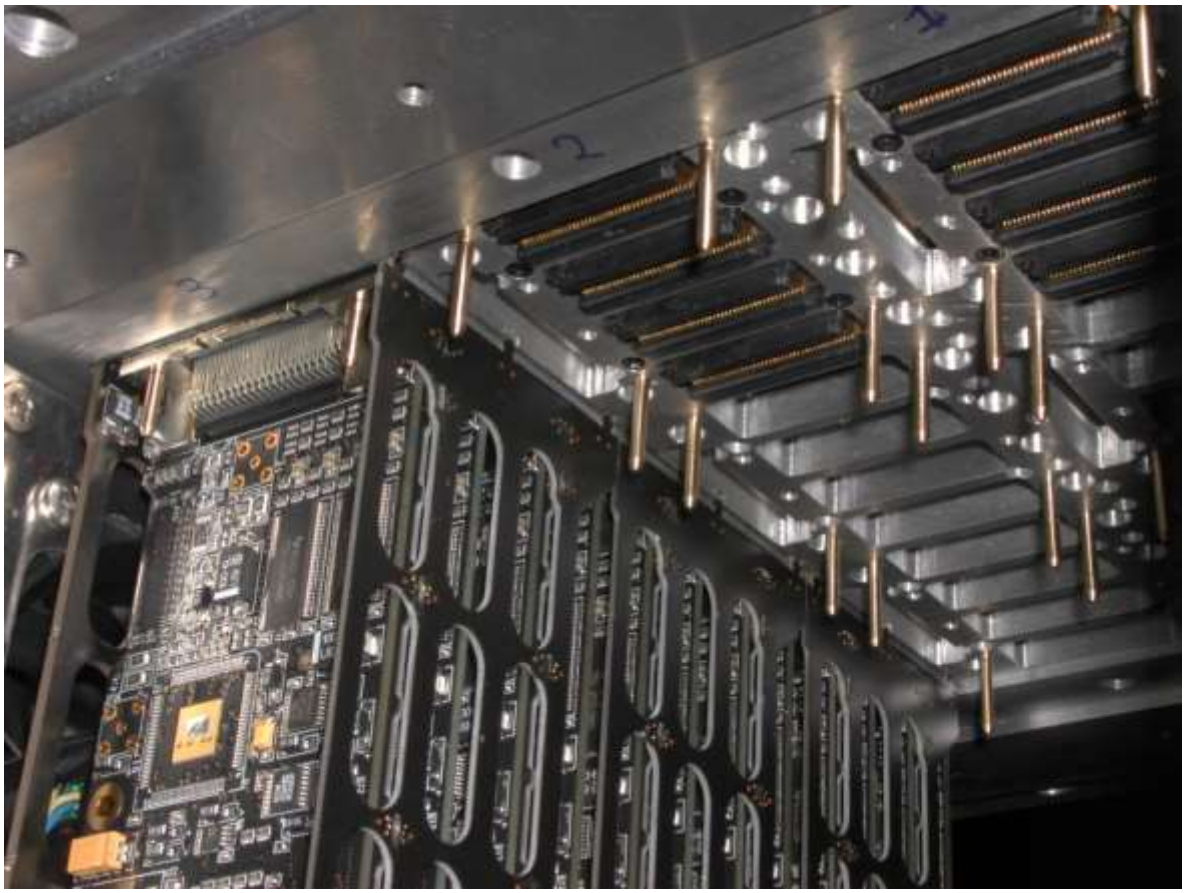

Figure 28. Row of 3 adjacent acquisition modules, inserted at the bottom of GAW focal plane front-end modules

Figure 29. GAW focal plane during assembly

Figure 30. GAW focal plane complete with 6 x 6 phototubes (36 units of 8x8 MAPMT = 2304 total pixels)